

AMENDMENTS TO THE CLAIMS

1. (Currently amended) An input level translator circuit comprising:
 - a first pass circuit that is coupled to a full-range node, to a first bias node, and to a high-range node;
 - a second pass circuit that is coupled to the full-range node, to a second bias node, and to a low-range node;
 - a first shunt circuit that is coupled between the first bias node and the high-range node; and
 - a second shunt circuit that is coupled between the second bias node and the low-range node,wherein the second shunt circuit is arranged to short the low-range node to the second bias node ~~includes a switch circuit that is arranged to close~~ if a voltage associated with the full-range node corresponds to a logic high.
2. (Previously Presented) An input level translator circuit comprising:
 - a first pass circuit that is coupled to a full-range node, to a first bias node, and to a high-range node;
 - a second pass circuit that is coupled to the full-range node, to a second bias node, and to a low-range node;
 - a first shunt circuit that is coupled between the first bias node and the high-range node; and
 - a second shunt circuit that is coupled between the second bias node and the low-range node,wherein
 - the first bias node and the second bias node have approximately the same voltage.
3. (Original) The input level translator circuit of claim 1, wherein
 - the first shunt circuit is configured to receive a first cascode bias voltage at the first bias node, wherein
 - the first cascode bias voltage is appropriate for biasing a cascode transistor.
4. (Original) The input level translator circuit of claim 1, wherein

7. (Original) The input level translator circuit of claim 6, wherein the second shunt circuit comprises a transistor that has:

a gate that is coupled to the full-range node,
a source that is coupled to the low-range node, and
a drain that is coupled to the second bias node.

8. (Currently amended) An input level translator circuit comprising:

a first pass circuit that is coupled to a full-range node, to a first bias node, and to a high-range node;

a second pass circuit that is coupled to the full-range node, to a second bias node, and to a low-range node;

a first shunt circuit that is coupled between the first bias node and the high-range node; and

a second shunt circuit that is coupled between the second bias node and the low-range node,

wherein the second shunt circuit is arranged to short the low-range node to the second bias node if a voltage associated with the full-range node corresponds to a logic high, and ~~The input level translator circuit of claim 1, wherein~~

the first shunt circuit is configured to influence a resistance between the first bias node and the high-range node depending on a full-range signal.

9. (Currently amended) An input level translator circuit comprising:

a first pass circuit that is coupled to a full-range node, to a first bias node, and to a high-range node;

a second pass circuit that is coupled to the full-range node, to a second bias node, and to a low-range node; and

a first shunt circuit that is coupled between the first bias node and the high-range node; ~~and~~

~~a second shunt circuit that is coupled between the second bias node and the low-range node,~~
wherein

the first shunt circuit is configured to isolate the first bias node from the high-range node if the full-range signal corresponds to a logic high, and to short the bias node to the high-range node if the full-range signal corresponds to a logic low.

10. (Previously Presented) An input level translator circuit comprising:

a first pass circuit that is coupled to a full-range node, to a first bias node, and to a high-range node;

a second pass circuit that is coupled to the full-range node, to a second bias node, and to a low-range node;

a first shunt circuit that is coupled between the first bias node and the high-range node; and

a second shunt circuit that is coupled between the second bias node and the low-range node, wherein

the first shunt circuit is configured to short the first bias node to the high-range node if the full-range signal corresponds to a logic low.

11. (Currently amended) An input level translator circuit comprising:

a first pass circuit that is coupled to a full-range node, to a first bias node, and to a high-range node;

a second pass circuit that is coupled to the full-range node, to a second bias node, and to a low-range node;

a first shunt circuit that is coupled between the first bias node and the high-range node; and

a second shunt circuit that is coupled between the second bias node and the low-range node,

wherein the second shunt circuit is arranged to short the low-range node to the second bias node if a voltage associated with the full-range node corresponds to a logic high, and ~~The input level translator circuit of claim 1, wherein~~

the second shunt circuit is configured to influence a resistance between the second bias node and the low-range node depending on a full-range signal.

12. (Original) The input level translator circuit of Claim 1, wherein

ensuring that the low range node is driven comprises influencing a resistance between a second bias node and the low-range node depending on the full-range signal.

16. (Original) The method of Claim 13, wherein

ensuring that the high-range node is driven comprises shorting the high-range node to the first bias node if the full-range signal corresponds to a first logic level; and

ensuring that the low-range node is driven comprises shorting the low-range node to the second bias node if the full-range voltage corresponds to the second logic level.

17. (Currently amended) ~~The~~ An input level translator circuit of Claim 10, wherein comprising:
the a-first pass circuit that is configured to provide a high-range signal at the a-high-range
node in response to a full-range signal;

the a-second pass circuit that is configured to provide a low-range signal at the a-low-range
node in response to the full-range signal;

~~a first shunt circuit that is coupled between a first bias node and the high range node,~~
~~wherein the first shunt circuit is configured to receive a p-type cascode bias signal at the first bias~~
~~node, wherein the first shunt circuit includes a switch circuit that is arranged to close if a voltage~~
~~associated with the full range node corresponds to a logic low; and~~

~~a second shunt circuit that is coupled between a second bias node and the low range signal,~~
wherein the second shunt circuit is configured to receive an n-type cascode bias signal at the second
bias node.

18. (Original) The input level translator circuit of claim 17, wherein

the full-range signal has a range from a low-voltage level to a high-voltage level,
the low-range signal has a range from the low-voltage level to an intermediate-voltage level,
the high-range signal has a range from the intermediate-voltage level to the high-voltage
level, and

the intermediate voltage level is partway between the low-voltage level and the high-voltage
level.

19. (Original) The input level translator circuit of claim 17, wherein the first shunt circuit is configured to:
- short the high-range node to the first bias node if the full-range signal corresponds to a first logic level, and
 - isolate the high-range node from the first bias node if the full-range signal corresponds to a second logic level, and
- the second shunt circuit is configured to:
- short the low-range node to the second bias node if the full-range signal corresponds to the second logic level, and
 - isolate the low-range node from the second bias node if the full-range signal corresponds to the first logic level.
20. (Currently amended) An apparatus for translating a level for a full-range signal, comprising:
- means for converting the full-range signal into a high-range signal at a high-range node;
 - means for converting the full-range signal into a low-range signal at a low-range node; and
 - means for ensuring that at least one of: the low-range node is driven during a full cycle of the full-range signal, or ~~and~~ the high-range node is driven during the full cycle of the full-range signal.